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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/494,787	01/31/2000	John A. Mount	SEA9274	3950

7590 07/16/2002

ATTEN: SHAWN B. DEMPSTER
SEAGATE TECHNOLOGY LLC
INTELLECTUAL PROPERTY DEPT. -SHK2LG
1280 DISC DRIVE
SHAKOPEE, MN 55379-1863

EXAMINER	
NGUYEN, MIKE	
ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 07/16/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/494,787	MOUNT, JOHN A.	
	Examiner	Art Unit	
	Mike Nguyen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-15 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-15 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawihgs are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Notices & Remarks

1. Claims 1-15 are pending for the examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Bowes et al. (U.S. Pat. No. 5,828,856).

4. As to claim 1, Bowes teaches in a storage system having a bus operatively coupled to a first controller chip and a first channel chip (see figure 2A elements 210, 222, 218 of the specification), the channel chip having several registers (see figure 3 elements 324, 314, 322, 312 316, 326, 366 of the specification), the storage system also having a storage medium operatively coupled to the bus through a storage medium interface (see figure 2A elements "Hard Disk

Drive", 214, 228 of the specification), a method for retrieving data record on a storage medium comprising the step of:

(a) retrieving a first portion of the record data via the bus (see figures 2A, 2B elements 244, 214, 210 and columns 5, lines 40-65, 1-13 of the specification, wherein a portion of the record data is retrieved by the DMA channel 244 via the I/O bus 214 or the CPU bus 210);

(b) updating some of the registers via the bus (see figure 3 elements 312, 322, 314, 324 and column 14 lines 29-35 of the specification, wherein some of the registers 312, 322, 314, 324 is updated after each transfer of the record data via the I/O bus 214 or the CPU bus 210); and

(c) retrieving a second portion of the record data via the bus (see figures 2A, 2B elements 244, 214, 210 and columns 5, 6 lines 40-65, 1-13 of the specification, wherein after retrieving the portion of the recorded data in (a) and updating some registers in (b) the DMA channel 244 will repeat the process if additional data in the bus needs to transfer).

5. As to claim 2, Bowes teaches the method of claim 1 in which the interface includes a read head (see column 7 lines 1-10 of the specification, wherein the interface has three control lines which carry the signals controlling whether the interface will be permitted to act. Therefore, it is obviously the interface containing a read head which is used to reposition), further comprising a step (d) of repositioning the storage medium interface with respect to the storage medium, between retrieving steps (a) and (c) (see figure 2B element 244 and column 6 lines 14-20 of the specification, wherein the position of the storage medium interface will be switched to another position with respect to the storage medium and DMA channel 244 will be repeatedly another transfer as claim 1).

6. As to claim 3, Bowes teaches the method of claim 2 in which the interface has plurality of operating parameters that are modified in updating step (b) (see figures 2B, 5 element 235 and columns 6, 7 lines 38-67, 1-20 of the specification, wherein the interface has plurality of operating parameters).

7. As to claim 4, Bowes teaches the storage system of claim 1 configured to perform the method of claim 1 in which the registers contain at least one read channel parameter value (see column 3 lines 8-20 of the specification, wherein the registers contain three channel parameter values) selected from the group consisting of: a precompensation value, a filter coefficient value, and a phase offset value (see column 5 lines 45-65 of the specification, wherein the values in a register are used to perform a read operation from I/O interface. The values in the register can be interpreted as "a precompensation value", "a filter coefficient value", and "a phase offset value").

8. As to claim 5, Bowes teaches the storage system of claim 1 configured to perform the method in which the registers contain at least one mode-indicative value (see figure 3 elements 316, 326, 320, 330 and columns 10, 12 lines 1-10, 40-50 respectively, wherein the registers 316, 326 contain at least one mode-indicative value which is used to reset the mode switch in response to a signal indicative of read or write).

9. As to claim 6, Bowes teaches in a storage system having a disc with at least two zones having zone identifiers Z_A and Z_B (see figure 2A. element "Hard disk drive" of the specification, wherein it is obviously the "Hard Disk Drive" containing at least two zones), an interface configured to read data in identifiers, a direct memory access (DMA) controller, a microprocessor coupled to the DMA controller (see figure 2A elements "Hard Disk Drive", 218,

222, 214, 210 of the specification), and several read channel registers each containing a value (see figure 3 elements 324, 314, 322, 312 316, 326, 366 of the specification), a method comprising steps of:

(a) retrieving via the DMA controller several indexed by zone identifier Z_B (see figures 2A, 2B elements 244, 214, 210 and columns 5, 6 lines 40-65, 1-13 of the specification respectively);

(b) updating at least some the read channel register values from the retrieved values (see figure 3 elements 312, 322, 324, 314 and column 14 lines 29-35 of the specification);

(c) reconfiguring the interface to read data in zone Z_B (see figure 2B element 235 and columns 5, 6 lines 55-65, 7-13 of the specification respectively, wherein the interface is repeatedly reconfigured to read data after the each update); and

(d) reading the target segment (see figures 2A, 2B elements 244, 214, 210 and columns 5, 6 lines 40-65, 1-13 of the specification respectively, wherein after reconfiguring the interface to read data the DMA channel 244 will again request access to read the target segment).

10. As to claim 7, Bowes teaches the method of claim 6 in which the target segment has a predetermined starting track number, further comprising a step of deriving zone identifier Z_B from the predetermined starting track number before retrieving step (a) (see figure 2B elements 250, 248 and columns 3, 12 lines 1-7, 35-62 of the specification respectively).

11. As to claim 8, Bowes teaches the method of claim 6 in which the interface includes at least one head (see column 7 lines 1-10 of the specification, wherein the interface has three control lines which carry the signals controlling whether the interface will be permitted to act. Therefore, it is obviously the interface containing a read head which is used to reposition), in

which positioning step (c) includes a step of (c1) moving the at least one head radically across the disc, the moving step (c1) beginning before retrieving step (a) is complete (see figure 2B elements 244, 214, 250, 224 and columns 5, 6 lines 60-65, 7-13 of the specification respectively).

12. As to claim 9, Bowes teaches the method of claim 8 in which moving step (c1) begins before retrieving step (a) begins (see figure 2B element 244 and column 6 lines 14-20 of the specification).

13. As to claim 10, Bowes teaches the method of claim 6 in which zone Z_B has a corresponding data rate R_B that is not in common with zone Z_A, in which positioning step (c) includes a step of (c2) sampling a signal from the interface at an initial frequency that is an integer multiple of data rate R_B (see figures 2A, 2B elements 218, 237, 244 and column 6 lines 29-36 of the specification).

14. As to claim 11, Bowes teaches the method of claim 6 further comprising prior steps of:

(e) configuring the interface to read data in zone Z_B (see figure 2B elements 210, 235, 248, 244, 283 and column 7 lines 14-20 of the specification);

(f) receiving a signal from the interface (see figure 2B elements 210, 235, 248, 244, 283 and column 7 lines 14-25 of the specification;

(g) deriving several values indicative of the interface's performance in zone Z_B from the received signal (see figure 2B element 235 and column 7 lines 34-47 of the specification); and

(h) storing some of the derived values in the value table each at a position associated with zone Z_B (see columns 7, 15 lines 39-43, 20-28 of the specification respectively).

15. As to claim 12, Bowes teaches the method of claim 6 in which the storage system includes an integrated circuit comprising the microprocessor, and in which the retrieving step (a) comprises issuing at least one but fewer than 10 commands from the microprocessor to the DMA controller (see figure 2A elements 222, 224, 226, 218 and columns 4, 5 lines 45-67, 1-21 of the specification respectively).

16. As to claim 13, Bowes teaches the method of claim 12 further comprising steps of:

(j) sensing position data from servo sector via the interface (see figures 2B, 5 elements 510, 512, 514, 235, 248, 250, 210 and column 7 lines 1-20 of the specification); and

(k) deriving a servo control signal from the sensed position data with the microprocessor during step (b) (see figures 2A, 2B elements 222, 210, 235 of the specification respectively).

17. As to claim 14, Bowes teaches the storage system of claim 6 configured to perform the method further comprising a printer circuit board assembly including a memory containing the value table, the storage system (see figure 2A elements 224, 226, 218, 222, "Hard Disk Drive" comprising:

a master integrated circuit (IC) containing the microprocessor and the direct memory access controller, the DMA controller being operatively coupled to the memory (see figure 2A elements 222, 218 224, 226 of the specification respectively);

a slave IC containing the several read channel registers; and a bus coupled between the master IC and the slave IC, the bus controllable by the DMA controller to perform updating step (b) (see figure 2A elements 224, 226, 210, 214 of the specification).

18. As to claim 15, Bowes teaches a disc drive comprising:

a disc stack comprising at least one disc (see figure 2A element "Hard Disk Drive" of the

specification);

an interface configured to read data from the at least one disc (see figure 2A element 214 of the specification);

a memory containing several values indexed by the zone identifier (see figure 2A elements 224, 226 of the specification, wherein it is obviously a memory containing several values);

a first controller chip containing a microprocessor and direct memory access (DMA) controller, the DMA controller operatively coupled to memory (see figure 2A elements 222, 218, 224, 226 of the specification);

a first channel chip having several registers (see figure 3 elements 324, 314, 322, 312, 316, 326, 366 of the specification); and

a bus operatively coupled between the interface and the chips, the bus controllable by the DMA controller to read from the memory and to update several of the registers in response to a zone transition event (see figure 2B elements 210, 235 244 of the specification).

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Bowes et al. (U.S. Pat No. 5,828,856)

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Nguyen whose telephone number is (703) 305-5040 or e-mail is mike.nguyen@uspto.gov. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:00 PM.

The appropriate fax number for the organization where this application or proceeding is assigned is (703) 746-7240.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Jeffrey Gaffin, can be reached on (703) 308-3301.

Any inquiry of a general nature or relating to the status of this application should be directed to the group receptionist whose telephone number is (703) 305-3900.

Mike Nguyen
Patent Examiner
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06/14/2002

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